

UNITED STATES PATENT APPLICATION

FOR

MULTIPLE USE OF MICROCONTROLLER PAD

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5 **MULTIPLE USE OF MICROCONTROLLER PAD**
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9 **CROSS REFERENCE TO RELATED DOCUMENTS**

10 This application is related to and claims priority benefit under 35
11 U.S.C. §119(e) of U.S. Provisional Patent Application Serial No. 60/243,708, filed
12 October 26, 2000 to Snyder, et al. which is hereby incorporated herein by
13 reference. This application is also related to U.S. Patent Application serial no.
14 _____ to Kutz, et al. entitled "Multiple Use of Microcontroller Pad", attorney
15 docket number CYPR-CD00231 which is hereby incorporated herein by reference.
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24 **FIELD OF THE INVENTION**

25 This invention relates generally to the field of integrated circuits. More
26 particularly, this invention relates to an arrangement for multiple use of wirebond
27 pads on a microcontroller die.
28

29 **BACKGROUND OF THE INVENTION**

1 In another embodiment, a microcontroller, consistent with the invention, has
2 a circuit including at least one of an analog circuit and a digital circuit. A wirebond
3 pad and a processor are arranged so that a switching circuit selectively connects
4 the circuit to the wirebond pad under control of the processor.
5

6 In certain preferred embodiments, the configurable analog circuit block has
7 an analog input and an analog output and the configurable digital circuit block has
8 a digital input and a digital output. The switching circuit selectively connects one
9 of the analog input, the analog output, the digital input and the digital output to the
10 wirebond pad under control of the processor. Various switching circuits including
11 tristate analog and digital circuits, analog switches and logic gates (for example)
12 can be used to effect the switching.

13 The above summaries are intended to illustrate exemplary embodiments of
14 the invention, which will be best understood in conjunction with the detailed
15 description to follow, and are not intended to limit the scope of the appended
16 claims.
17

18 BRIEF DESCRIPTION OF THE DRAWINGS

19 The features of the invention believed to be novel are set forth with
20 particularity in the appended claims. The invention itself however, both as to
21 organization and method of operation, together with objects and advantages
22 thereof, may be best understood by reference to the following detailed description
23 of the invention, which describes certain exemplary embodiments of the invention,
24 taken in conjunction with the accompanying drawings in which:

25 **FIGURE 1** is an exemplary layout of an integrated circuit die.

26 **FIGURE 2** is an overall block diagram of a microcontroller consistent with
27 an exemplary embodiment of the present invention.

28 **FIGURE 3** illustrates a first switching arrangement for configuring a wirebond
29 pad consistent with an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be recognized by one skilled in the art that the present invention may be practiced without these specific details or with equivalents thereof. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will herein be described in detail specific embodiments, with the understanding that the present disclosure is to be considered as an example of the principles of the invention and not intended to limit the invention to the specific embodiments shown and described. In the description below, like reference numerals are used to describe the same, similar or corresponding parts in the several views of the drawings.

Turning now to **FIGURE 1**, an integrated circuit die 10 is illustrated. Die 10 includes a plurality of wirebonding pads 14 (which are typically used for providing a wirebond or soldered electrical connection to the integrated circuit) situated around a periphery of the die 10. The pads 14 are separated by a separation distance 22 defined generally by the resolution of the circuit's manufacturing process and the circuit layout. Pads 14 are shown symmetrically disposed around the periphery in this illustration, but this is not generally a requirement. The pads 14 are also generally of a particular geometry, generally square with a minimum size 26 as shown, but other shapes are also used.

In the classic manufacturing process, an array of such dice are produced on a wafer of silicon. The dies are then separated from one another by cutting or breaking at a scribe line. During this process, the corner areas 30 of the die have historically been exposed to substantial amounts of mechanical stress and may fracture or break in the separation process. However, gradual improvements in the

1 technology of separation of the dies has substantially lessened the stress and
2 incidence of fractures in this region.

3 In order to maximize the versatility of the circuit arrangement of the present
4 invention, a microcontroller 100 as illustrated in **FIGURE 2** utilizes one or more
5 multi-purpose pads 114. Microcontroller 100 includes a processor 120 that can be
6 programmed for a specified purpose by or for a user. A plurality of digital circuits
7 are provided to form configurable digital blocks 124. These configurable digital
8 blocks 124 can include gates, counters, buffers, latches, decoders, encoders,
9 registers, flip-flops, timers, etc. that can be user configured in any suitable
10 arrangement to implement a user's desired circuit configuration. Similarly, a
11 plurality of analog circuits are provided to form configurable analog blocks 130.
12 These configurable analog blocks may include filters, amplifiers, switches, clippers,
13 limiters, summers, buffers, etc. that can be interconnected in a suitable
14 arrangement to implement the user's desired circuit configuration.

15 The inputs and outputs for the configurable digital blocks 124 and
16 configurable analog blocks 130 are coupled to a plurality of configurable switches
17 136 to be routed to the multi-purpose pad 114. These switches are programmed
18 by the user or at manufacture through the processor 120 and can be arranged in
19 a number of ways to provide multiple use of the pad 114 to provide a uni-directional
20 or bi-directional signal path as illustrated. The switching arrangement illustrated
21 in **FIGURE 2** is somewhat conceptual and can be implemented in any number of
22 ways as illustrated in **FIGURES 3-6** as well as other implementations that will
23 occur to those skilled in the art.

24 **FIGURE 3** illustrates a first circuit arrangement that can be utilized to
25 implement the switching function of configurable switches 136. In this
26 embodiment, an electronic switch circuit 304 can be used. Switch circuit 304 can
27 be realized with, for example, a plurality of CMOS analog switches with one side
28 of each switch connected together at a common junction. Switch 304 is connected
29 to an analog input 310, an analog output 314, a digital input 320 and a digital output

1 326 - any of which can be connected to pad 114 depending upon the switch
2 position. The switch position can be determined by a control bus 330 that serves
3 to enable one of the desired connections (e.g., by selectively turning on one of the
4 CMOS analog switches) and thus complete the circuit to pad 114. The switch can
5 be configured under the control of the processor 120 as either analog or digital,
6 input or output.

7 In another embodiment illustrated in **FIGURE 4**, an analog input (to the
8 microcontroller through pad 114) can be selectively switched to 310 using an
9 analog switch 404 operating under control of an analog in enable control line 410
10 that turns switch 404 on or off as desired to implement a connection to pad 114.
11 An analog output from the microcontroller 100 can be selectively provided using
12 tristate buffer amplifier 414. The analog out signal at 314 to be supplied to pad 114
13 is supplied to the non-inverting input of a voltage follower configured operational
14 amplifier. The amplifier can be selectively enabled using tristate control at a tristate
15 analog out enable line 420. Tristate control can similarly be used to control
16 digital out signal 326 through a tristate inverter 424. The output of the tristate
17 inverter 424 is connected to pad 114 and it can be effectively removed from the
18 circuit or switched on using tristate control applied by tristate digital out enable
19 signal 430 to control whether or not the inverter is enabled or "tri-stated". Tristate
20 control can similarly be used to control digital in signal 320 through a tristate
21 inverter 436. The high impedance input of the tristate inverter 436 is connected to
22 pad 114 and it can be effectively removed from the circuit or switched on using
23 tristate control applied by tristate digital in enable signal 440 to control whether or
24 not the inverter is enabled or disabled (tri-stated). In this embodiment, the pad 114
25 is isolated from the circuitry within the microcontroller by the high impedance of a
26 tristate controlled gate or an analog switch in the off position to thus prevent
27 unnecessary loading. Again, the switching arrangement can be configured under
28 the control of the processor 120 as either analog or digital, input or output.

29 **FIGURE 5** illustrates another embodiment of a switching arrangement

1 consistent with the present invention. In this embodiment, resistors are used to
2 provide isolation to reduce circuit complexity. An analog input signal to the
3 microcontroller 100 passes from pad 114 through an isolation resistor 510 to
4 provide the input at node 310. If the input is not being used as an analog input, the
5 signal at 310 is simply ignored by the microcontroller 100 or not connected to a
6 functioning configurable analog circuit block 130. As in the example of **FIGURE 5**,
7 an analog output from the microcontroller 100 can be selectively provided using
8 tristate buffer amplifier 414. The analog out signal 314 to be supplied to pad 114
9 is supplied to the non-inverting input of a voltage follower configured operational
10 amplifier. The amplifier can be selectively enabled using tristate control at a tristate
11 analog out enable line 420.

12 In this embodiment, digital NAND gates are used for switches in the digital
13 signal paths. Other digital gates such as AND gates could also be used. NAND
14 gate 520 is used to gate a signal from digital out 326 to pad 114 through an
15 isolation resistor 526. The pad 114 is configured as a digital output by use of a
16 digital signal applied to digital out enable 530 to either pass or reject digital signals
17 at node 326. A logic zero at 530 effectively forces the output of NAND gate 520 to
18 a logic high state at all times to effectively turn off the gate. Resistor 526 isolates
19 this high state from the pad 114. Other isolation resistor arrangements could also
20 be used. In a similar manner, NAND gate 540 is used to gate a signal from pad
21 114 to digital in 320 through an isolation resistor 546. The pad 114 is configured
22 as a digital input by use of a digital signal applied to digital in enable 550 to either
23 pass or reject digital signals at pad 114. A logic zero at 550 effectively forces the
24 output of NAND gate 540 to a logic high state at all times. Again, the switching
25 arrangement can be configured under the control of the processor 120 as either
26 analog or digital, input or output.

27 Another embodiment is illustrated in **FIGURE 6**. In this embodiment, as in
28 **FIGURE 5**, an analog input signal to the microcontroller 100 passes from pad 114
29 through an isolation resistor 510 to provide the input at node 310. If the input is not

1 being used as an analog input, the signal at 310 is simply ignored by the
2 microcontroller 100 or not connected to a functioning configurable analog circuit
3 block 130. As in **FIGURE 4**, tristate control is used to control digital out signal 326
4 through a tristate inverter 424. The output of the tristate inverter 424 is connected
5 to pad 114 and it can be effectively removed from the circuit or switched on using
6 tristate control applied by tristate digital out enable signal 430 to control whether
7 or not the inverter is enabled or tri-stated.

8 Analog output signals can be passed to pad 114 by use of an analog buffer
9 configured operational amplifier 610. The input of amplifier 610 is connected to
10 analog out node 314 and the output is passed through an analog switch 614 to pad
11 114. A digital signal at 620 controls the state of switch 614 to provide an analog
12 out enable function. Switch 614 provides isolation between the amplifier 610's
13 output and pad 114 if the analog out function is not enabled. In another
14 embodiment, not shown, a resistor could be used for isolation in place of switch
15 614 with no input being applied to the amplifier 314. Digital input signals can be
16 accommodated by use of an inverter (or buffer) 630 with its input connected to pad
17 114. The inverter's output is provided as a signal at node 320. In this embodiment,
18 the inverter has no tristate control or other switching mechanism as such and the
19 output of inverter 630 is simply not connected to functional logic or ignored if not
20 being used. Again, the switching arrangement can be configured under the control
21 of the processor 120 as either analog or digital, input or output.

22 Other switching arrangements can also be provided without departing from
23 the invention using switches, tristate devices, logic switches and other switching
24 arrangements to provide selective control by the processor of the configuration of
25 one or more pads of microcontroller to thus enhance the versatility of the device
26 without increasing device size to accommodate numerous pinouts. Moreover,
27 although specific combinations of switching techniques have been illustrated with
28 each example of **FIGURES 3-6**, the switching techniques shown for each signal
29 line can be used individually in any suitable combination to provide the switching

1 most suitable to a given application, circuit manufacturing process, layout, etc. In
2 addition, although analog inputs were only shown switched using an analog switch,
3 a tristate amplifier buffer could also be used as in the case of analog outputs. Also,
4 while NAND gates were used as switches, other multiple input logic gates could
5 be used. And, although inverting tristate buffers were used as switches, non-
6 inverting configurations could also be used. Moreover, although only a single
7 connection (e.g., analog or digital input or output) has been described as connected
8 to the wirebond pad under microcontroller control, multiple connections to a single
9 pad can also be implemented within the scope of the present invention. Such
10 variations should be considered equivalents.

11 While the invention has been described in conjunction with specific
12 embodiments, it is evident that many alternatives, modifications, permutations and
13 variations will become apparent to those skilled in the art in light of the foregoing
14 description. Accordingly, it is intended that the present invention embrace all such
15 alternatives, modifications and variations as fall within the scope of the appended
16 claims.

17 What is claimed is:
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